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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/747,779	12/22/2000	Hong Koo Kim	000939073311	4408

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EXAMINER

PIZARRO CRESPO, MARCOS D

ART UNIT PAPER NUMBER

2814

DATE MAILED: 05/20/2003

13

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action

Application No.

09/747,779

Applicant(s)

KIM, HONG KOO

Examiner

Marcos D. Pizarro-Crespo

Art Unit

2814

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 29 April 2003 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE. Therefore, further action by the applicant is required to avoid abandonment of this application. A proper reply to a final rejection under 37 CFR 1.113 may only be either: (1) a timely filed amendment which places the application in condition for allowance; (2) a timely filed Notice of Appeal (with appeal fee); or (3) a timely filed Request for Continued Examination (RCE) in compliance with 37 CFR 1.114.

PERIOD FOR REPLY [check either a) or b)]

- a) ☒ The period for reply expires 3 months from the mailing date of the final rejection.
- b) ☐ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection. ONLY CHECK THIS BOX WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

1. ☐ A Notice of Appeal was filed on _____. Appellant's Brief must be filed within the period set forth in 37 CFR 1.192(a), or any extension thereof (37 CFR 1.191(d)), to avoid dismissal of the appeal.
2. ☐ The proposed amendment(s) will not be entered because:
- (a) ☐ they raise new issues that would require further consideration and/or search (see NOTE below);
 - (b) ☐ they raise the issue of new matter (see Note below);
 - (c) ☐ they are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
 - (d) ☐ they present additional claims without canceling a corresponding number of finally rejected claims.

NOTE: _____

3. ☐ Applicant's reply has overcome the following rejection(s): _____.
4. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
5. ☒ The a) ☐ affidavit, b) ☐ exhibit, or c) ☒ request for reconsideration has been considered but does NOT place the application in condition for allowance because: see Continuation below.
6. ☐ The affidavit or exhibit will NOT be considered because it is not directed SOLELY to issues which were newly raised by the Examiner in the final rejection.
7. ☐ For purposes of Appeal, the proposed amendment(s) a) ☐ will not be entered or b) ☐ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

The status of the claim(s) is (or will be) as follows:

Claim(s) allowed: _____.

Claim(s) objected to: _____.

Claim(s) rejected: _____.

Claim(s) withdrawn from consideration: _____.

8. ☐ The proposed drawing correction filed on _____ is a) ☐ approved or b) ☐ disapproved by the Examiner.
9. ☐ Note the attached Information Disclosure Statement(s) (PTO-1449) Paper No(s). _____.
10. ☐ Other: _____

Continuation of 5.

does NOT place the application in condition for allowance.


The applicant argues:

Claim 1 recites a step of thermally annealing the buffer layer to enhance the alignment of crystallites of the layer. In one embodiment, this is accomplished by annealing an MgO buffer layer for about 30 minutes at a temperature of 800-1000°C (see, e.g., specification/pp. 7/11.9-16). At the same time, this annealing step facilitates the growth of a highly-oriented ferroelectric layer on the buffer layer. Hirai (see, e.g., col. 7/11.37-43) differently heats the substrate to form a silicon oxide layer underneath the buffer layer 5. The heating step of Hirai appears to be different than the claimed annealing step, reflecting the differences in intended purpose of the two steps. That is, Hirai's heating step is performed at a temperature of 650-750°C for 5-20 minutes, whereas the claimed annealing step is performed at a temperature of 800-1000°C for about 30 minutes. It may be possible that different parameters than those disclosed in the specification may enhance the alignment of crystallites of the buffer layer. However, one would have to appreciate the need for such a step to formulate a different set of parameters. Hirai does not disclose or suggest such an appreciation.

The examiner responds:

A limitation in a claim with respect to the manner in which a claimed method step is intended to be used does not differentiate the claimed process from the prior-art process if the process in the prior art teaches all the step limitations in the claim unless the intended use resulted in a manipulative difference as compared to the prior art. In re Casey, 152 USPQ 235 (CCPA 1967); In re Otto, 136 USPQ 458, 459 (CCPA 1963). In the above argument, the applicant states that there is a manipulative difference implied in the intended use of the annealing step. In his statement the applicant incorporates the limitations of claim 13 as reading in the intended use of the annealing step. That is, in order to enhance the alignment of crystallites of the buffer layer, the annealing step should be performed at a temperature of 800-1000°C for about 30 minutes (claim 13). However, as stated in the rejection of claim 13 in the previous Office action in paper no. 11 and as the applicant points out in the above argument, Hirai teaches that the annealing step may be performed at 750°C for 20 minutes (see, e.g., Hirai/col. 7/11.37-43). Also in paper no. 11, the examiner stated that although Hirai fails to specify the exact claimed temperature and time, differences in temperature and time will not support the patentability of subject matter encompassed by the prior art unless there is evidence indicating such parameters as critical or as achieving unexpected results (see paragraph 27 in paper no. 11). Far from establishing either the critical nature or any unexpected results arising from the specified temperatures and time the applicant states that "it may be possible that different parameters than those disclosed in the specification may enhance the alignment of crystallites of the buffer layer". The applicant continues to say that "one would have to appreciate the need for such a step to formulate a different set of parameters". However, it has been held that the reference may suggest doing what an applicant has done even though those of ordinary skill in the art were ignorant of the existence of the problem (In re Gershon, 152 USPQ 602 (CCPA 1967)). In the instant case, Hirai clearly teaches about the importance of keeping the crystallites in the buffer layer aligned. For example, Hirai teaches that the lack of control at the interface between a Si substrate and a ferroelectric layer creates problems from the standpoint of reproducibility and stability of a ferroelectric nonvolatile memory (see, e.g., Hirai/col. 1/11.60-col. 2/11.9). Like the applicants, Hirai teaches that an oriented buffer layer, of which MgO is also an example (see, e.g., col. 4/11.6), is needed to facilitate the control and growth of a highly-oriented ferroelectric layer on the buffer layer (see, e.g., col. 4/11.30-35). This oriented buffer layer is also required for preventing the deterioration of the ferroelectric layer (see, e.g., col. 4/11.62-67). Hirai specifies that the oriented buffer layer has the crystallites aligned in a fixed direction (see, e.g., col. 3/11.53-57). The annealing step that Hirai discloses in col. 7/11.37-43 is performed before the ferroelectric layer is formed. Accordingly, the annealing step that Hirai discloses in col. 7/11.37-43 must ensure the alignment of the crystallites within the buffer layer, even more so, since the step is performed before the ferroelectric layer is formed.

All other arguments presented by the applicants have been considered and addressed in a previous Office action.


LONG PHAM
PRIMARY EXAMINER